CLAIMS

What is claimed is:

1. A semiconductor device assembly, comprising:

a carrier substrate comprising a substantially planar structure with a surface including at least one first contact area thereon, proximate at least one opening formed through said carrier substrate; and

a solder mask comprising at least one opening through which said at least one opening and said at least one first contact area of said carrier substrate are exposed.

2. The semiconductor device assembly of claim 1, further comprising:

at least one semiconductor die secured to another surface of said carrier substrate opposite said surface thereof, at least one bond pad of said at least one semiconductor die being exposed through said at least one opening of said solder mask and said at least one opening of said carrier substrate.

3. The semiconductor device assembly of claim 2, further comprising:

at least one intermediate conductive element extending between said at least one bond pad and said at least one first contact area.

4. The semiconductor device assembly of claim 3, wherein a thickness of said solder mask exceeds a height said at least one intermediate conductive element protrudes above said surface of said carrier substrate.

5. The semiconductor device assembly of claim 3, further comprising:

a quantity of encapsulant material within said at least one opening of said carrier substrate and said at least one opening of said solder mask.

6. The semiconductor device assembly of claim 5, wherein an upper surface of said quantity of encapsulant material is substantially level with an outer surface of said solder mask.

7. The semiconductor device assembly of claim 5, wherein a distance between an uppermost portion of said at least one intermediate conductive element and an outer surface of said solder mask is at least about 25 μm.

8. The semiconductor device assembly of claim 7, wherein said at least one intermediate conductive element comprises a bond wire and a thickness of said solder mask is equal to the sum of a distance a portion of a loop of said bond wire protrudes above said surface of said carrier substrate and about 25 μm.

9. The semiconductor device assembly of claim 1, wherein said carrier substrate includes at least one second contact area on said surface thereof and at least one conductive trace electrically connecting said at least one first contact area and said at least one second contact area.

10. The semiconductor device assembly of claim 9, wherein said at least one second contact area is at least partially exposed through an aperture of said solder mask.

11. The semiconductor device assembly of claim 10, further comprising:
at least one discrete conductive element protruding from said at least one second contact area above said solder mask.

12. The semiconductor device assembly of claim 11, wherein at least half of a height of said at least one discrete conductive element protrudes above an outer surface of said solder mask.

13. The semiconductor device assembly of claim 1, wherein said solder mask comprises a material with a coefficient of thermal expansion substantially the same as a material of said carrier substrate.

14. The semiconductor device assembly of claim 1, wherein said solder mask comprises a cured photoimageable material.

15. The semiconductor device assembly of claim 1, wherein a thickness of said solder mask is about 50 μm to about 100 μm.